AMENDMENT TO THE CLAIMS

1. (currently amended) A method of encoding digital information in order to suppress direct current (dc) content , the method comprising :

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receiving a sequence of m message bits of a message word; ~~and~~

mapping the sequence of m message bits of the message word to a codeword, of length n bits, generated from the m message bits using algebraic operations~~.~~, wherein mapping the sequence of m message bits further comprises:

generating a plurality of codeword candidates, each of length n bits, from the m message bits using algebraic operations; and

selecting one of the plurality of codeword candidates based upon an optimizing criteria.

2. (canceled)

3. (original) The method of claim 2, wherein generating the plurality of codeword candidates further comprises generating each of the plurality of codeword candidates by adding a different one of a plurality of periodic scrambling sequences to the m message bits of the message word.

4. (original) The method of claim 3, wherein selecting one of the plurality of codeword candidates further comprises generating second order digital sum sequences corresponding to each of the plurality of codeword candidates, and selecting the one of the plurality of codeword candidates based upon the second order digital sum sequences.

5. (original) The method of claim 4, wherein each of the plurality of codeword candidates is a binary sequence, and wherein selecting one of the plurality of codeword candidates further comprises

converting the bipolar sequence of each codeword candidate to a bipolar sequence.

6. (original) The method of claim 5, wherein for the bipolar sequence corresponding to each of the plurality of codeword candidates, selecting one of the plurality of codeword candidates further comprises:

generating a first order running digital sum for the codeword candidate;

determining a set of positions within the codeword candidate, such that, modifying the codeword candidate by inverting bits in the codeword candidate starting at a position from the set of positions results in a running digital sum for the codeword candidate being equal to zero; and

calculating a separate second order running digital sum sequence for the codeword candidate and each respective position in the corresponding set of positions within the codeword candidate at which bit inversion began.

7. (original) The method of claim 6, wherein calculating the separate second order running digital sum sequence for the codeword candidate and each respective position in the corresponding set of positions within the codeword candidate further comprises calculating the second order running digital sum sequences for each of the plurality of codeword candidates and for each respective position in the corresponding set of positions at which bit inversion began as cumulative sums of first order running digital sum values.

8. (original) The method of claim 7, wherein selecting one of the plurality of codeword candidates further comprises selecting the one of the plurality of codeword candidates and the position in the corresponding set of positions which produces the smallest absolute

value of second order running digital sum, together with the periodic scrambling sequence which was added to it.

9. (original) The method of claim 8, and before receiving the sequence of m message bits of a message word , further comprising modulating the message word with an error correcting code to provide the sequence of m message bits.

10. (original) The method of claim 8, and after mapping the sequence of m message bits of the message word to the codeword, further comprising modulating the codeword with an error correcting code.

11. (original) An encoding apparatus which encodes digital information in order to suppress direct current (dc) content, the encoding apparatus comprising:

an input receiving a sequence of m message bits of a message word;

a plurality of parallel processing branches each generating a different codeword candidate from the m message bits using algebraic operations; and

a selector for selecting one of a plurality of codeword candidates, each generated by a different one of the plurality of parallel processing branches, based upon an optimizing criteria.

12. (original) The encoding apparatus of claim 11, wherein each of the plurality of parallel processing branches comprises scrambling circuitry which receives the m message bits and a scrambling sequence as inputs and provides as an output a codeword candidate, wherein the scrambling sequence used by each processing branch is different than the scrambling sequence used by all of the others of the plurality of parallel processing branches.

13. (original) The encoding apparatus of claim 12, wherein each of the plurality of parallel processing branches further comprises conversion circuitry coupled to the scrambling circuitry, the conversion circuitry converting the codeword candidate from a binary sequence to a bipolar sequence.

14. (original) The encoding apparatus of claim 13, wherein each of the plurality of parallel processing branches further comprises:

first order running digital sum calculating circuitry, coupled to the conversion circuitry to generate a first order running digital sum for the codeword candidate having the bipolar sequence;

inversion position determining circuitry coupled to the first order running digital sum circuitry to determine a set of positions within the codeword candidate, such that, modifying the codeword candidate by inverting bits in the codeword candidate starting at a position from the set of positions results in a running digital sum for the codeword candidate being equal to zero; and

a plurality of running digital sum registers storing a running digital sum sequence for the codeword candidate and each respective position in the corresponding set of positions within the codeword candidate at which bit inversion began.

15. (original) The encoding apparatus of claim 14, wherein each of the plurality of parallel processing branches further comprises second order running digital sum calculating circuitry coupled to the plurality of running digital sum registers to calculate a separate second order running digital sum sequence for the codeword candidate and each respective position in the corresponding set of positions within the codeword candidate at which inversion begins.

16. (original) The encoding apparatus of claim 15, wherein the selector is coupled to the plurality of parallel processing branches and selects the one of a plurality of codeword candidates and the position in the corresponding set of positions which produces the smallest absolute value of the second order running digital sum, together with the corresponding scrambling sequence.

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17. (currently amended) An apparatus for encoding digital information in order to suppress direct current (dc) content , the apparatus comprising:

an input which receives a sequence of m message bits of a message word; and

means for mapping the sequence of m message bits of the message word to a codeword, of length n bits, generated from the m message bits using algebraic operations~~.~~ by generating a plurality of codeword candidates and selecting one of the plurality of codeword candidates based upon an optimizing criteria.

18. (new) The apparatus of claim 17, wherein the means for mapping comprises:

a plurality of parallel processing branches each generating a different codeword candidate from the m message bits using algebraic operations; and

a selector for selecting one of a plurality of codeword candidates, each generated by a different one of the plurality of parallel processing branches, based upon an optimizing criteria.

19. (new) The apparatus of claim 18 wherein, each of the plurality of parallel processing branches comprises scrambling circuitry which receives the m message bits and a scrambling sequence as

inputs and provides as an output a codeword candidate, wherein the scrambling sequence used by each processing branch is different than the scrambling sequence used by all of the others of the plurality of parallel processing branches.

20. (new) The apparatus of claim 19, wherein each of the plurality of parallel processing branches further comprises conversion circuitry coupled to the scrambling circuitry, the conversion circuitry converting the codeword candidate from a binary sequence to a bipolar sequence.

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21. (new) The apparatus of claim 20, wherein each of the plurality of parallel processing branches further comprises:

first order running digital sum calculating circuitry, coupled to the conversion circuitry to generate a first order running digital sum for the codeword candidate having the bipolar sequence;

inversion position determining circuitry coupled to the first order running digital sum circuitry to determine a set of positions within the codeword candidate, such that, modifying the codeword candidate by inverting bits in the codeword candidate starting at a position from the set of positions results in a running digital sum for the codeword candidate being equal to zero; and

a plurality of running digital sum registers storing a running digital sum sequence for the codeword candidate and each respective position in the corresponding set of positions within the codeword candidate at which bit inversion began.